GLAST ACD Front End ASIC : GAFE

Electronics Review

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Introduction

- This presentation describes the Front End Analog Electronics ASIC for GLAST ACD

Topics of Discussion

- ASIC Requirements
- ASIC Architecture & Description
- Pin out and Interfacing
- Test results & Simulations
- Test Plan
- Future Iterations
- Revisions

ASIC Requirements

- Primary Objective: To generate a fast VETO Trigger signal for GLAST ACD
- Secondary Objective: To Pulse Height Analysis (PHA) of the PMT signal

ASIC Requirements:
Detector

- PMT gain = 400,000
- Anode_output (negative charge) to process signals in the range 0.1 MIP to 1000 MIPS

ASIC Requirements:
Input Charge Range

- 0.1 MIP to 1000 MIPs
- dynamic range = 1 : 10,000
- 0.1 MIP <=> 1 Photo electron (pe) <=> 1.6 E-19 Coulombs
- dynamic range = 1.6E-19 C to 1.6E-15 C
- Since the gain of the PMT is 400,000, the charge input to the ASIC is as:
- 0.064PC for 0.1 MIP
- 0.64 PC for 1 MIP
- 640 PC for 1000 MIPs.

ASIC Requirements:
VETO Generation

- Generate a trigger output for signals above a nominal threshold of 0.3MIPs
- VETO Threshold**:** Adjustable from 0.1 MIP to 2 MIP with a step size of 0.05 MIP or a charge range of 0.064pc to 1.28pc with a step size of 0.032PC
- Veto Trigger Latency: latency for the entire ACD electronics chain within 600ns, the minimum latency expected is 150ns and is not likely to be less than 50ns. The jitter on the Veto trigger shall be less than or equal to 200 ns.
- VETO Duration: longer than the time for baseline recovery to 0.05 MIP
- Recovery to 1 MIP: For 1 MIP signal, VETO should be no longer than 1.2us
- Recovery to Large Signals (1000 MIPs): VETO should be no longer than 10 us
- VETO Signal Retrigger: To be retriggerable within 50ns of the trailing edge.

ASIC Requirements:
PHA Requirements

- **PHA (Pulse Height Analysis) output:**
- Low Energy / High Gain Channel:

  (Range: 0 to 10 Mips)

  - Resolution: 0.1 MIP to 10 MIPs with a precision of 0.02 MIP or 5% which ever is larger
- High Energy / Low Gain Channel:

  (Range: 0 to 1000 Mips)

  - Resolution : for pulses above 20 MIPs and upto 1000 MIPs, a precision of 1 MIP or 2% which ever is larger

ASIC Requirements:
CNO or HLD Trigger

- **CNO or HLD or High Level Threshold Detection:** nominal threshold of 25 MIPs
- **CNO or HLD Threshold:** Adjustable from 20 to 64 MIPs in steps of less than or equal to 1MIP
- **CNO or HLD Latency:** latency no more than that of VETO signal.

ASIC Requirements:
LLD or ZS Trigger

- No longer required but still provided on the ASIC
- nominal threshold of 0.1 MIP
- LLD or ZS Threshold: Adjustable from 0.05 MIP to 1 MIP in steps of 0.05 MIP

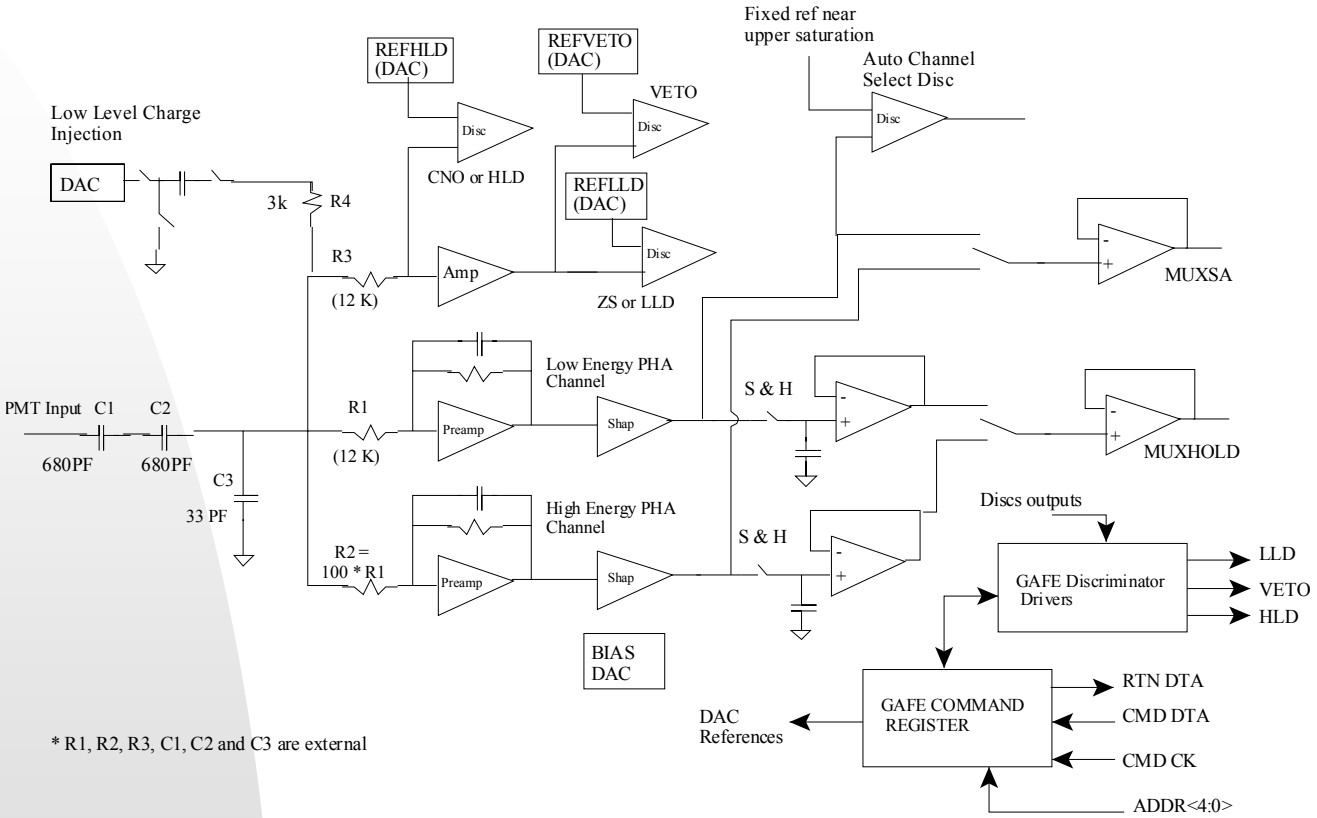
ASIC Requirements:
Test Charge Injection

- ASIC to have mechanism for injecting test charge at the front end of electronics chain, the maximum injected charge will be 40pc (16pf * 2.5v), which corresponds to 62.5 MIPs.

ASIC Requirements:
Event Rate

- < 3 KHz per PMT
- <= 5% of PMTs are expected to be digitized on an average

ASIC Architecture



GLAST ACD Front End (GAFE) Analog ASIC : Conceptual Diagram

ASIC Architecture

Salient Features

The dynamic range of 0.1 to 1000 MIP which for a PMT gain of 400,000 translates to 0.064 PC to 640 PC, this is a dynamic range of 1:10,000

Generation of a fast VETO trigger, preferably within 200ns for a 1 MIP signal

The desired peaking time for the PHA signal is 3us, a shorter time is not desirable as it will lead to greater errors due to timing jitter of the Sample Hold signal.

ASIC Architecture

Charge Splitting

- The large dynamic range of 0.1 to 1000 Mips is handled by splitting the input charge into two channels.
- Charge splitting accomplished by 2 resistances with a ratio of 1:100

ASIC Architecture

Input Time Const / VETO Duration

- VETO signal be 1 us for 1 MIP
- 0.1 mip = 1 mip * exp(-1us/tau)

=> tau = 0.43 us

ASIC Architecture

Shaping for PHA

- Latency of Hold from LAT = 2us
- To accommodate 20% tolerances in R and C, the minimum Peaking Time has been increased to 3us
- Error due to timing jitter is small for larger shaping time

ASIC Architecture

Sample and Hold

- The sample and hold comprises of a simple switch in series with the output of the final stage of shaping amplifier and a hold capacitor as shown in fig. 1. During normal operation, the switch is kept closed and the voltage across the hold capacitor tracks the output of the shaping amplifier, and when the hold signal is applied the signal across the capacitor is held.

ASIC Architecture

Analog Multiplexed Outputs

- Multiplexed Shaped Amp output
  (used only for Testing, not in flight)
- Multiplexed Sample & Hold Output

ASIC Architecture

Fast Channel Amplifier

- Input to VETO and LLD Discriminators amplified by 20
- This is advantageous for reliable triggering and to keep the trigger delays small

ASIC Architecture

Test Charge Injection

- An on chip capacitor of approximately 16 Pf has been fabricated, for a 2.5 v input, this would allow charge injection of 40 PC or 62.5MIPs. When not needed, the charge injection capacitor is disconnected by a switch that is activated by the Test Enable signal.

ASIC Architecture

PMT Gain Drift

- HV increased so that the gain of the weakest PMT is acceptable
- Adjust the threshold of discriminators for each channel individually
- Paralleling of charge cap at the ASIC input

ASIC Architecture
DACS : Overview

- The DACs are used to set the discriminator threshold as follows :

Signal	Min Setting	Max Setting	Step Size	No. of Bits
Veto	0 MIP	3.2 MIPs	0.05 MIP	6 bits
LLD	0 MIP	3.2 MIP	0.05 MIP	6 bits
HLD	0 MIP	64 MIPs	1 MIP	6 bits

ASIC Architecture

DACS : Disc Base Line

- This is a fixed level generated by the DAC block and is set to 1.75 v, the signal going into all the discriminators have a dc offset of this value of 1.75 v.
- The signal going into the discriminators is an inverted exponential in shape, and therefore the various thresholds are set below this baseline.

ASIC Architecture

DACS : Shaping Base Line

- Base Line DAC is a 3 bit DAC that sets the baseline at the output of the Shaping Amps between 2.2 v and 1.75 v, the nominal setting is 2v.

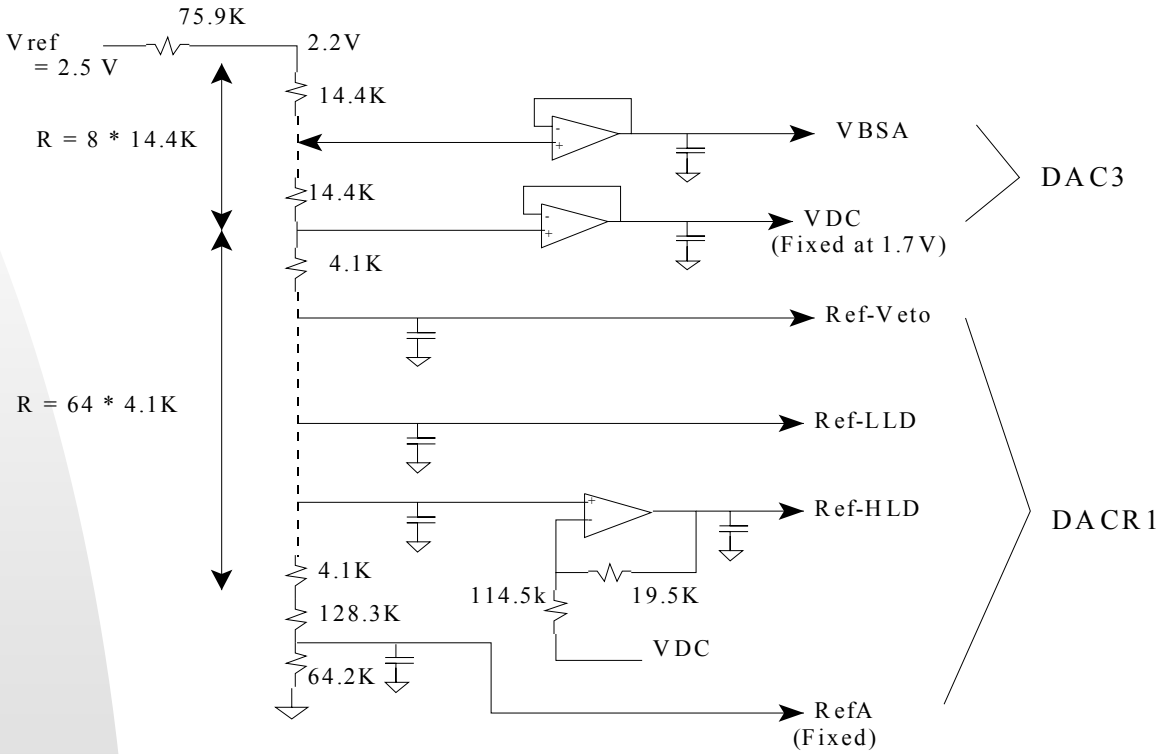
ASIC Architecture

DACS : Auto Channel Disc

- This is a fixed level and is set to 0.8V. When the signal in the low energy channel has exceeded the difference between this voltage and the DC base line at the shaping amp out, then the auto channel discriminator fires and this is used to switch the PHA to the high energy channel.

ASIC Architecture

DACS : Architecture



An Overview of the DAC architecture in GAFE ASIC

ASIC Pin Out:
Power Pins

- VCC : 2 Pins
- AGND: 7 pins
- Vdd: 2 pins
- DGND : 3pins

ASIC Pin Out:
Analog Pins

- Salo & Sahi: Low & High energy inputs
- Dsicin: Fast channel input for discriminators
- Muxh, muxsa: multiplexed hold and shap amp outputs

ASIC Pin Out:
Digital Pins

- All disc outputs are low volt differential signals
- HLD is output as 2 terms of a switch to implement a common OR
- Clock, command, data, sample & Hold, Test charge injection: All signals are LVDS

ASIC Prototypes Developed

- Built and Tested and the core analog modules in SOI Tech : French Dmill process
- Built and Tested and the core analog modules in SOI Tech : Peregrine process
- Currently Testing the prototype in Ag/HP 0.5um CMOS

ASIC Tools Used

- Magic and Tanner
- Simulation using Spice
- Verification by LVS and simulation after extraction

Test Plans

- Test the current prototypes with Vector boards
- Build a PCB for large scale testing of ASICs
- The Test PCB will interface with the GARC Test PCB
- The data will be collected through the GARC Test PCB
- Special Software for Testing to be written

Summary

- The ASIC requirements, Design and Test results were presented